Amendment to the Title:

Please replace the title of the description as originally filed with the following new title:

RECEIVER OF ANALOGUE VIDEO SIGNAL HAVING MEANS FOR ANALOGUE VIDEO SIGNAL CONVERSION AND METHOD FOR CONTROL OF DISPLAY OF VIDEO FRAMES

Amendment to the Specification:

► Please amend paragraph 3 as follows:

[Para 3] The present invention relates to a ~~device for control of display of video frames~~ receiver of analogue video signal having means for analogue video signal conversion and a method for control of display of video frames, used in digital decoders/receivers of television signal, in which the signal is received in an analogue form, and then, after conversion into a digital signal, it is processed in the decoder/receiver (e.g. OSD 'On-Screen Display' functions are applied). Next it is converted to an analogue format, which is transmitted to a receiver, for example a TV set.

► Please amend paragraph 13 as follows:

[Para 13] A ~~device for control of display of video frames~~ receiver of analogue video signal having means for analogue video signal conversion, according to the present invention, comprises a receiving block for receiving a first analogue video signal or an input video signal, a conversion block for conversion of the first analogue signal, of a first format, into a digital signal and connected to the receiving block, a buffer controller of frame buffers, connected to the conversion block, the buffer controller comprising three modules, (a) buffers linked together, (b) a decoding frame controller and (c) a displaying frame controller, a video coder for transforming the output digital signal into an output analogue signal or an analogue signal of a second format, a receiver for displaying the analogue signal of a second

format and a processor for data processing and controlling the receiving block, the conversion block, the buffer controller, the video coder and the receiver.

► Please amend paragraph 19 as follows:

[Para 19] In the accompanying drawings one of the possible embodiments of the present invention is shown, where:

Fig. 1 is a typical analogue video signal;

Fig. 2 is a schematic diagram of a ~~device for control of display of video frames~~ receiver of analogue video signal having means for analogue video signal conversion;

Fig. 3 is a shift of video frame synchronizing signals;

Fig. 4 is a flow chart of a procedure of decoding signal frames;

Fig. 5 is a flow chart of a procedure of displaying signal frames;

Fig. 6 is a flow chart of a procedure of organizing video signal frame buffers;

Fig. 7 is a diagram of steps of fetching and displaying of frames when an input frequency is higher than an output frequency; and

Fig. 8 is a diagram of steps of fetching and displaying of frames when an input frequency is lower than an output frequency.

► Please amend paragraph 21 as follows:

[Para 21] A ~~device for control of display of video frames~~ receiver of analogue video signal having means for analogue video signal conversion, for which the method of controlling

display of video frames described in the present invention is intended, is shown in Fig. 2. This ~~device~~ receiver is a television signal receiver/decoder, which fetches television data from an analogue video signal. A receiving block 201 of the analogue video signal transmits data read from the analogue signal to a conversion block 202, where conversion of the analogue signal into a digital signal takes place. After the conversion, data are transmitted to a buffers controller 203, which consists of a decoding controller 203a, buffers 203b and a displaying controller 203c. The buffer controller 203 controls writing of the data in the buffers 203b, reading of the data from the buffers 203b and transmitting the data form the buffers 203b to a video coder 204, which transforms the digital signal into an analogue signal, which is next transmitted to a receiver 205, for example a television set. The whole process of data processing is controlled by the processor 206 of the television receiver/decoder. In addition, data can be further processed in the buffers.

► Please amend paragraph 24 as follows:

[Para 24] A flow chart of a procedure of decoding frames is shown in Fig. 4. This procedure controls decoding of a picture frame and writing it ~~the~~ to the selected frame buffer. The procedure starts in step 401. Its first task, in step 402, is to set the current decoder buffer - to which the data will be decoded – to the first buffer on a list of frame buffers. In the next step 403, the procedure awaits for a bottom vertical synchronization signal in the input video signal. When the controller detects such signal, the procedure moves to step 404, where a check is made, whether the buffer, next in relation to the current buffer of the decoder, is being displayed. This prevents the overwriting of the data composing the currently displayed

video frame. If it is not displayed, the current decoder buffer, to which the data will be written, is set in step 405 to the next buffer and the procedure moves to step 406. In the opposite case, when the next buffer is being displayed, there is a direct shift to step 406, where - after detecting the signal of the top vertical synchronization in the analogue input signal data - decoding to the current decoder buffer the takes place. Finally the procedure proceeds to step 403 and further operates in a loop.

► Please amend paragraph 26 as follows:

[Para 26] Frame buffers - with cyclically recorded data - are shown in Fig. 6. They are organized as a two-way list, where each buffer 602 contains, in addition to the given video frame, a pointer 603 to the next buffer in the two-way list, and a pointer 601 to the previous buffer from the two-way list. As shown in the drawing, there is also a connection between the first buffer and the last buffer in the two-way list. An input 604 to the frame buffers is defined by the decoder buffer pointer set according to the procedure described with reference to Fig. 4 and an output 605 from the frame buffers is defined by the display buffer pointer set according to the procedure described with reference to Fig. 5. The input 604 and the output 605 are managed by the decoding controller 203a and the displaying controller 203c respectively.